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PATENT
Customer No. 22,852
Attorney Docket No. 7447.0021-01
Xerox Ref. No. D/99215D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
LU, Jeng Ping et al.	)	Group Art Unit: 2815
	)	
Application No.: 10/067,424	)	Examiner: LANDAU, Matthew
	)	
Filed: February 7, 2002	)	
	)	
For: DUAL DIELECTRIC STRUCTURE FOR SUPPRESSING LATERAL LEAKAGE CURRENT IN HIGH FILL FACTOR ARRAYS	)	Confirmation No.: 8498

MAIL STOP APPEAL BRIEF-PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

In reply to the Notification of Non-Compliant Appeal Brief mailed July 23, 2007,

Applicant Submits an Amended Appeals Brief and the following Remarks.

REMARKS

Applicants filed an Appeal Brief on June 14, 2007, in response to the Office Action mailed on November 15, 2006 and pursuant to 37 C.F.R. 41.31. The Notice of Appeal was originally filed on February 14, 2007. On July 23, 2007, the Office mailed a Notification of Non-Compliant Appeal Brief ("Notification"). In response, Applicants are submitting an Amended Appeal Brief with this paper which cures the issues raised by the Notification.

In particular, the Examiner has pointed out the following alleged deficiencies:

1) In the Status of Claims, the examiner states that "This section should list the status of all the claims involved in the application. This section should also explicitly identify the claims involved in the appeal.

2) In the Summary of Claims Subject Matter, the examiner states that "The independent claims 7, 11 and 16 should be mapped to the specification by page and line number, paragraph number, or to the drawings, if any.

3) In the Appendices, the Evidence Appendix and Related Proceedings are missing. The Examiner insists that if nothing is to be submitted, an indication of "None" is required.

In response to paragraph 1 above, Applicant's Amended Appeal Brief provides explicitly a list of the status of the claims in the Status of the Claims and to clarifies that the rejected status of claims 7-14 and 16-19 are being appealed.

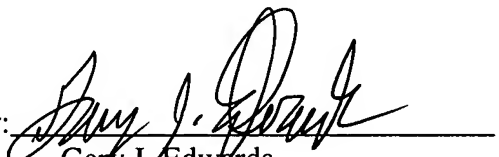
In response to paragraph 2 above, Applicant's Amended Appeal Brief provides a table specifically mapping each of the claim elements to a portion of the specification that discusses that element.

In response to paragraph 3, above, Applicants Amended Appeal Brief now includes Appendix E, the Evidence Appendix, and Appendix F, the Related Proceedings Appendix, both explicitly stating that nothing is to be submitted.

To the extent any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this response, such extension is hereby respectfully requested. If there are any additional fees due that are not enclosed, please charge such fees to our Deposit Account No. 24-0037.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

By: 
Gary J. Edwards
Reg. No. 41,008

Dated: August 23, 2007

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PATENT
Customer No. 22,852
Attorney Docket No. 7447.0021-01
Xerox PARC Ref. No. D/99215D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
LU, Jeng Ping et al.	)	Group Art Unit: 2815
	)	
Application No.: 10/067,424	)	Examiner: RICHARDS, N. Drew
	)	
Filed: February 7, 2002	)	
	)	Confirmation No.: 8498
For: DUAL DIELECTRIC STRUCTURE FOR SUPPRESSING LATERAL LEAKAGE CURRENT IN HIGH FILL FACTOR ARRAYS	)	

MAIL STOP: APPEAL BRIEF-PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDED APPEAL BRIEF

Sir:

Appellant appeals the rejection of claims 7-14 and 16-19 in the Office Action mailed on November 15, 2006 ("Office Action"). Appellant filed a Notice of Appeal and the fee set forth in 37 C.F.R. § 41.20(b)(1) on February 14, 2007. Applicant subsequently filed an Appeal Brief and the fee set forth in 37 C.F.R. § 41.20(b)(2) on June 14, 2007. Appellant requests the Board of Appeals to reverse in whole the rejection of claims 7-14 and 16-19 and order the allowance of these claims.

I. Real Party in Interest

The real party in interest is Xerox Corporation.

II. Related Appeals and Interferences

There are no related appeals or interferences at this time.

III. Status of Claims

Claims 7-14 and 16-19 are pending in this application and stand rejected. Claims 1-6 and 15 have been canceled. The status of the claims are listed as follows:

Claims 1-6 are canceled;

Claims 7-14 are rejected;

Claim 15 is canceled; and

claims 16-19 are rejected.

Applicants appeal the rejection of claims 7-14 and 16-19. Appealed claims 7-14 and 16-19 are reproduced in Appendix A for the Board's convenience.

IV. Status of Amendments

There are no outstanding amendments in this application.

V. Summary of Claimed Subject Matter

Applicant's invention is directed to a method of forming a full fill-factor image array with greatly enhanced suppression of lateral leakage current by including duel dielectric passivation layers between adjacent metal contacts of the image array. As illustrated in Figure 3 (reproduced here as Appendix C) of the specification, in general a full fill-factor image array according to the Applicant's invention can be formed by providing a plurality of source-drain metal contacts (144) on a substrate (42); depositing a first passivation layer (156) over the plurality of source-drain metal contacts; depositing a second passivation layer (157), which significantly reduces the resulting lateral leakage current between optically active collection electrodes, over the first passivation layer, the second passivation layer being thinner than the first passivation layer; opening via holes through the first and second passivation layers to the

plurality of source-drain metal contacts; depositing a layer of conductive material (146) over the plurality of source-drain metal contacts and the second passivation layer; depositing a doped alpha-Si layer (148) over the layer of conductive material; patterning the alpha-Si layer and the layer of conductive material to form collection electrodes; depositing a layer of intrinsic amorphous silicon (150) over the second passivation layer and the alpha-Si layer; and depositing a conductive layer over the intrinsic amorphous silicon layer.

Claims 7-14 and 16-19 recite various aspects of this method. Claim 7 is directed to a method of making a high fill factor image array according to the present invention. As recited in claim 7, the method includes providing a plurality of source-drain metal contacts on a substrate; depositing a first passivation layer over the plurality of source-drain metal contacts and the substrate; reducing the lateral leakage current between the plurality of source-drain metal contacts in the high fill factor image array by depositing a second passivation layer over the first passivation layer, the second passivation layer being thinner than the first passivation layer; opening a plurality of via holes through the first and second passivation layers to the plurality of source-drain metal contacts; depositing a layer of conductive material over the plurality of source-drain metal contacts and the second passivation layer; depositing a first doped a-Si layer as an optically active layer over the layer of conductive material; patterning the first doped a-Si layer and the layer of conductive material to form collection electrodes; depositing a continuous layer of intrinsic amorphous silicon on the second passivation layer and the first doped amorphous silicon layer; depositing a second layer of doped amorphous silicon over the continuous layer of intrinsic amorphous silicon; depositing an upper conductive layer over the second layer of doped amorphous silicon; and patterning to form the image array. Once formed,

the high fill-factor image array exhibits much lower lateral leakage currents than those that utilize a single passivation layer between optically active elements.

Claims 8-10 depend from claim 7. Claim 8 provides the further limitation that the first passivation layer is formed of silicon oxynitride, BCB, or a polyimide, which as suggested in the specification are low dielectric constant materials that are low stress. Claim 9 provides the further limitation that the second passivation layer is an oxide. Claim 10 provide that the thickness of the second passivation layer be about 1000 Å.

Claim 11 is directed to the structure of a high fill-factor array that is formed by substantially the process recited in claim 7. Claims 12-14, which are dependent from claim 11, are substantially similar to claims 8-10, respectively.

Claim 16 is of similar scope as Claim 7. Claim 16 differs from claim 7 at least in that it is focused on formation of a single optically active element of the full fill-factor array rather than on the entire array. Claims 17-19, which depend from claim 16, are similar to claims 8-10 and claims 12-14.

The claims of the application, then, are generally directed to formation of a full fill-factor array that includes a first passivation layer and a second passivation layer located between optically active elements where the second passivation layer has the effect of reducing the lateral leakage current between optically active elements. An explicit mapping of independent claims 7, 11, and 16 to the specification and drawings is provided below:

Claim Element	**Reference**
7. A method for making a high fill factor image array comprising the	The method is illustrated in Figures 5a through 5d and discussed on page 8, line 8, through page 9, line 16. Figure 3 illustrates an

steps:	embodiment of the completed structure.
providing a plurality of source-drain metal contacts on a substrate;	Figure 3, which shows two of source drain metal contact 144. Figure 5a also shows the source drain metal contact 144. A discussion of the source drain contact 144 with respect to Figure 5a is on page 8, lines 10-13. Substrate 42 is shown in Figure 3, but not illustrated in Figures 5a through 5d.
depositing a first passivation layer over the plurality of source-drain metal contacts and the substrate;	Figure 3 shows a first passivation layer 156. Deposition of first passivation layer 156 is discussed, with respect to Figure 5a, at page 8, lines 10-17.
reducing the lateral leakage current between the plurality of source-drain metal contacts in the high fill factor image array by depositing a second passivation layer over the first passivation layer, the second passivation layer being thinner than the first passivation layer;	Figure 3 shows a second passivation layer 157. Figure 5a illustrates the second passivation layer 157 over the first passivation layer. Deposition of the second passivation layer, which is less than that of the first passivation layer, is discussed on page 8, line 18, through page 9, line 2. The reduction in lateral leakage current is discussed with respect to Figure 4 on page 7, line 15, through page 8, line 7.

opening a plurality of via holes through the first and second passivation layers to the plurality of source-drain metal contacts;	Via 160, which is positioned over the source drain metal contact 144, is shown in Figure 5b and discussed in the specification at page 9, lines 3-4.
depositing a layer of conductive material over the plurality of source-drain metal contacts and the second passivation layer;	Conductive material 146, which is deposited over the source drain metal contacts 144 and second passivation layer 157, is shown in Figure 3 and in Figure 5c and discussed in the specification at page 9, lines 5-6.
depositing a first doped a-Si layer as an optically active layer over the layer of conductive material;	The first doped a-Si layer 148 is shown in Figure 3 and Figure 5c and deposition of this layer is discussed in the specification at lines 7-8. As discussed in the specification at page 2, lines 15-18, i a-Si layer 148 is a photosensitive element.
patterning the first doped a-Si layer and the layer of conductive material to form collection electrodes;	Patterning first doped a-Si layer 148 and conductive material 146 is shown in Figure 5c and discussed in the specification at page 9, lines 7-10.
depositing a continuous layer of i a-Si disposed on the second passivation	Depositing i a-Si layer 150 on second passivation layer 157 and first doped a-Si layer

layer and the first doped a-Si layer;	148 is illustrated in Figure 5d and discussed in the specification at page 9, line 11. The i a-Si layer is also shown in Figure 3 and discussed in the specification at page 6, line 20, through page 7, line 2.
depositing a continuous second layer of doped a-Si over the continuous layer of i a-Si;	Depositing second doped a-Si layer 152 is also illustrated in Figure 5d and discussed in the specification at page 9, line 12-13. The second doped a-Si layer 152 is also shown in Figure 3 and discussed on page 7, line 1, of the specification.
depositing an upper conductive layer over the second layer of doped a-Si; and	Depositing upper electrode 154 is illustrated in Figure 5d and discussed in the specification at page 9, lines 13-16. Upper electrode 154 is also shown in Figure 3 and discussed in the specification at page 7, lines 1-2.
patterning to form the image array.	Patterning to form the image array is discussed in the specification at page 9, lines 15-16.
11. A high fill factor image array formed by:	A high fill factor image array is illustrated in Figure 3 and discussed in the specification on page 6, line 13, through page 8, line 7. A

	method of forming the high fill factor image array is illustrated in Figures 5a-5d and discussed in the specification at page 8, line 8, through page 9, line 16.
providing a plurality of source-drain metal contacts on a substrate;	Figure 3, which shows two of source drain metal contact 144. Figure 5a also shows the source drain metal contact 144. A discussion of the source drain contact 144 with respect to Figure 5a is on page 8, lines 10-13. Substrate 42 is shown in Figure 3, but not illustrated in Figures 5a through 5d.
depositing a first passivation layer over the plurality of source-drain metal contacts and the substrate;	Figure 3 shows a first passivation layer 156. Deposition of first passivation layer 156 is discussed, with respect to Figure 5a, at page 8, lines 10-17.
reducing the lateral leakage current between the plurality of source-drain metal contacts in the high fill factor image array by depositing a second passivation layer over the first passivation layer, the second passivation layer being thinner	Figure 3 shows a second passivation layer 157. Figure 5a illustrates the second passivation layer 157 over the first passivation layer. Deposition of the second passivation layer, which is less than that of the first passivation layer, is discussed on page 8, line 18, through page 9, line 2. The reduction in lateral leakage

than the first passivation layer;	current is discussed with respect to Figure 4 on page 7, line 15, through page 8, line 7.
opening a plurality of via holes through the first and second passivation layers over the plurality of source-drain metal contacts;	Via 160, which is positioned over the source drain metal contact 144, is shown in Figure 5b and discussed in the specification at page 9, lines 3-4.
depositing a layer of conductive material on the plurality of source-drain metal contacts and over the second passivation layer;	Conductive material 146, which is deposited over the source drain metal contacts 144 and second passivation layer 157, is shown in Figure 3 and in Figure 5c and discussed in the specification at page 9, lines 5-6.
depositing a first doped a-Si layer as an optically active layer over the layer of conductive material;	The first doped a-Si layer 148 is shown in Figure 3 and Figure 5c and deposition of this layer is discussed in the specification at lines 7-8.
patterning the first doped a-Si layer and the layer of conductive material to form collection electrodes;	Patterning first doped a-Si layer 148 and conductive material 146 is shown in Figure 5c and discussed in the specification at page 9, lines 7-10.
depositing a continuous layer of i a-Si disposed on the second passivation	Depositing i a-Si layer 150 on second passivation layer 157 and first doped a-Si layer

layer and over the first doped a-Si layer;	148 is illustrated in Figure 5d and discussed in the specification at page 9, line 11. The i a-Si layer is also shown in Figure 3 and discussed in the specification at page 6, line 20, through page 7, line 2.
depositing a continuous second layer of doped a-Si over the continuous layer of i a-Si;	Depositing second doped a-Si layer 152 is also illustrated in Figure 5d and discussed in the specification at page 9, line 12-13. The second doped a-Si layer 152 is also shown in Figure 3 and discussed on page 7, line 1, of the specification.
depositing an upper conductive layer over the continuous second layer of doped a-Si; and	Depositing upper electrode 154 is illustrated in Figure 5d and discussed in the specification at page 9, lines 13-16. Upper electrode 154 is also shown in Figure 3 and discussed in the specification at page 7, lines 1-2.
patterning to form the image array.	Patterning to form the image array is discussed in the specification at page 9, lines 15-16.
16. A method for making a high fill factor image array comprising:	The method is illustrated in Figures 5a through 5d and discussed on page 8, line 8, through page 9, line 16. Figure 3 illustrates an

	embodiment of the completed structure.
providing a source-drain metal contact;	Figure 3, which shows two of source drain metal contact 144. Figure 5a also shows the source drain metal contact 144. A discussion of the source drain contact 144 with respect to Figure 5a is on page 8, lines 10-13.
depositing a first passivation layer over the source-drain metal contact;	Figure 3 shows a first passivation layer 156. Deposition of first passivation layer 156 is discussed, with respect to Figure 5a, at page 8, lines 10-17.
reducing the lateral leakage current between the plurality of source-drain metal contacts in the high fill factor image array by depositing a second passivation layer over the first passivation layer, the second passivation layer being thinner than the first passivation layer;	Figure 3 shows a second passivation layer 157. Figure 5a illustrates the second passivation layer 157 over the first passivation layer. Deposition of the second passivation layer, which is less than that of the first passivation layer, is discussed on page 8, line 18, through page 9, line 2. The reduction in lateral leakage current is discussed with respect to Figure 4 on page 7, line 15, through page 8, line 7.
opening a via hole through the first and second passivation layers to expose	Via 160, which is positioned over the source drain metal contact 144, is shown in Figure 5b

the source-drain metal contact;	and discussed in the specification at page 9, lines 3-4.
depositing a layer of conductive material on the source-drain metal contact, such that the layer of conductive material makes electrical contact with the source-drain metal contact;	Conductive material 146, which is deposited over the source drain metal contacts 144 and second passivation layer 157, is shown in Figure 3 and in Figure 5c and discussed in the specification at page 9, lines 5-6.
depositing a first doped a-Si layer as an optically active layer on the layer of conductive material;	The first doped a-Si layer 148 is shown in Figure 3 and Figure 5c and deposition of this layer is discussed in the specification at lines 7-8.
patterning the a-Si layer and the layer of conductive material to form a collection electrode;	Patterning first doped a-Si layer 148 and conductive material 146 is shown in Figure 5c and discussed in the specification at page 9, lines 7-10.
depositing sensor material comprising a continuous layer of i a-Si over the collection electrode and at least a porition of the second passivation layer;	Depositing i a-Si layer 150 on second passivation layer 157 and first doped a-Si layer 148 is illustrated in Figure 5d and discussed in the specification at page 9, line 11. The i a-Si layer is also shown in Figure 3 and discussed

	in the specification at page 6, line 20, through page 7, line 2. As discussed in the specification at page 2, lines 15-18, i a-Si layer 148 is a photosensitive element.
depositing a continuous layer of doped a-Si over the continuous layer of i a-Si;	Depositing second doped a-Si layer 152 is also illustrated in Figure 5d and discussed in the specification at page 9, line 12-13. The second doped a-Si layer 152 is also shown in Figure 3 and discussed on page 7, line 1, of the specification.
depositing a conductive layer over the continuous layer of doped a-Si; and	Depositing upper electrode 154 is illustrated in Figure 5d and discussed in the specification at page 9, lines 13-16. Upper electrode 154 is also shown in Figure 3 and discussed in the specification at page 7, lines 1-2.
patterning conductive layer to form an upper electrode.	Patterning to form the image array is discussed in the specification at page 9, lines 15-16.

VI. Grounds of Rejection to Be Reviewed on Appeal

A. Whether claims 7-14 and 16-19 should be rejected under 35 U.S.C. § 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) in view of Ishaque et al. (U.S. Patent No. 5,288,989) and Possin et al. (U.S. Patent No. 5,777,355).

VII. Argument

In the office action mailed on November 15, 2006, the Examiner re-iterated the rejection of claims 7-14 and 16-19 under 35 U.S.C. § 103 (a) over the AAPA in light of Ishaque and Possin. As is discussed below, the Examiner erred in this rejection. Claims 7-14 and 16-19 are allowable over this prior art.

Applicants have pointed out to the Examiner that the system described in Ishaque is substantially different than that described and claimed in the present application. Ishaque teaches

> [a]n avalanche photodiode (APD) [that] has a two tier passivation layer disposed over the silicon APD body. The passivation layer includes an inorganic moisture barrier layer and an organic dielectric layer.

(Ishaque, abstract). The structure of the optical device described in Ishaque is substantially different from that described and claimed in the present application. As shown in the Figure of Ishaque, the optically active element 120 is deposited directly on a transparent conductive contact pad 110. Optically active element 120 is formed in mesas with beveled sidewalls sloping upward and inwardly from the bottom contact pad towards the upper surface. Dual passivation layer 130, having passivation layers 132 and 134, is deposited over the optically active element 120. Contact 140 is then formed in contact with optically active portion 120 at contact area 126 through a via formed in passivation layers 132 and 134. During operation, light is incident on the device through transparent conductive contact pad 110 and detected in optically active area 120.

Dual passivation layer 130 is, then, open to atmospheric conditions. The teachings of Ishaque, then, is mainly directed towards application of a moisture barrier layer 134 on top of

passivation layer 132. As taught in Ishaque, the moisture barrier layer protects the APD from damage due to diffusion of water vapor.

Ishaque does discuss leakage current in general, but not specifically lateral leakage current. (*See* Ishaque, col. 6, line 32, through col. 7, line 2). Further, Ishaque teaches that embodiments where the dielectric barrier layer is deposited over the moisture barrier layer had worse leakage current characteristics than where the dielectric barrier layer is deposited on the device and the moisture barrier layer is deposited over the dielectric barrier layer. (*See* Ishaque, col. 6, lines 45-51). However, as is further taught by Ishaque, the lower leakage current is specifically attributable to the dielectric barrier layer being in contact with the underlying silicon material. As taught in Ishaque

> For example, in otherwise similar nine-element arrays, measured leakage current was 10 nA for the arrangement in which the organic dielectric 132 was disposed immediately adjacent to APD body 120, and 30 nA in the embodiment in which the inorganic dielectric was disposed immediately adjacent to APD body 122. This improved array performance, that is lower noise, arises from the low leakage of APDs fabricated in accordance with this invention. Factors that are thought to result in the lower noise in APDs having the organic dielectric layer adjacent to the silicon body include improved adherence between the organic material (polyimide, for example) and the silicon (as opposed to the adherence of the silicon to the inorganic moisture barrier, such as silicon nitride); smaller trap states at the silicon surface for the organic dielectric in contact with the silicon of APD body 120 as opposed to the silicon nitride in contact with the silicon of the APD body; and curing the organic material at a high temperature before the application of the inorganic moisture barrier obviates the need to expose the inorganic material to high temperatures that tend to cause cracks or structural degradation of the inorganic material.

(Ishaque, col. 6, lines 45-68). As a result, as Ishaque teaches, the reduction in leakage current is caused by the organic dielectric being in contact with the underlying silicon. The second

passivation layer of Ishaque has little to do with leakage current, and is provided as a moisture barrier.

In contrast, the reduction in lateral leakage current in Applicant's invention results from the replacement of a single passivation layer with the dual passivation layer structure. The second passivation layer does not function as a moisture barrier, which would have no function in these passivation layers because these passivation layers are buried within the structure of the device and are not exposed to atmosphere. However, as is described in the specification and recited in the claims, providing a two-tiered passivation layer in place of the single passivation layer in the structure of the prior art full fill-factor array as shown in Figure 2, reduces the lateral leakage current over the effect of having the single passivation layer alone.

As described in Applicant's specification, and illustrated in Figure 2 (reproduced here as Appendix B), a full fill-factor array with a single passification layer is known. Again, Applicant's invention is directed towards substitution of a two-tiered passivation layer for the single passivation layer, which has the effect of reducing the lateral leakage current between elements of the array, as is shown in Figure 4 (reproduced here as Appendix D) of the Applicant's specification.

Possin teaches another radiation imager that utilizes a moisture passivation layer in order to prevent moisture from penetrating the device. As taught in Possin, "[d]egradation due to exposure to moisture can make sidewall leakage a significant leakage source in almost any size photodiode." (Possin, col. 1, lines 43-45). Accordingly, Possin teaches a structure, as is shown in Figure 2 of Possin, where a gate dielectric layer 18 is disposed between two adjacent bottom contacts 14. A bottom passivation layer 22 is then disposed over the gate dielectric layer 18 and the semiconductor material of the photodoide, 13 and 113. A polymer bridge layer 24 is then

disposed between and over portions of adjacent diodes and common electrode 28 is disposed on the bridge layer 24. Finally, barrier layer 30 then overlies the array of photodiodes. Possin teaches that the common electrode 28 can be patterned to form the detector array. (*See,* Possin, col. 3, lines 45-65). However, the second passivation layer is deposited over the top only after such patterning is accomplished. The second passivation layer, barrier layer 30, is a moisture barrier layer to protect the image array from atmospheric damage. Therefore, Possin, like Ishaque, only teaches utilization of a second passivation layer as a moisture barrier and utilizes a single passivation layer to reduce leakage current.

The Examiner has not established a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* M.P.E.P. § 2142, 8th Ed., Rev. 5 (August 2006). Moreover, "in formulating a rejection under 35 U.S.C. § 103(a) based upon a combination of prior art elements, it remains necessary to identify the reason why a person of ordinary skill in the art would have combined the prior art elements in the manner claimed." USPTO Memorandum from Margaret A. Focarino, Deputy Commissioner for Patent Operations, May 3, 2007, page 2. As is discussed below, the combination of the art cited by the Examiner (i.e., Ishaque, AAPA, and Possin) does not teach all of the elements of the claims. Further, one skilled in the art would not combine these references as suggested by the Examiner.

I. The cited prior art does not teach all of the elements of the claims.

1. None of the references teach "reducing the lateral leakage current . . . ."

None of the references teach "reducing the lateral leakage current between the plurality of source-drain metal contacts in the high fill factor image array by depositing a second passivation layer over the first passivation layer," as is recited in claims 7, 11, and 16.

As the Examiner has previously admitted "the AAPA does not discuss using a second passivation layer overlying the first passivation layer to prevent the conducting channels from forming between two pixel electrodes" (Office Action mailed March 4, 2003, pgs 2-3). Ishaque teaches "[a]n avalanche photodiode (APD) [with] a two tier passivation layer disposed over the silicon APD body." (Ishaque, abstract). Ishaque teaches that "an avalanche photodiode (APD) includes an APD body, a bottom contact pad, a top contact pad, and a two-tier passivation layer." (Ishaque, col. 3, lines 26-29). As further taught in Ishaque, "[t]he two-tier passivation layer is disposed over the APD body so as to cover the outer periphery of the APD body except at a selected contact area with the top contact." (Ishaque, col. 3, lines 42-45). Ishaque does teach the effect on the leakage current of reversing the order of the dielectric layer and the moisture barrier layer. (Ishaque, col. 6, line 32-col. 7, line 2). However, Ishaque does not discuss lateral leakage current or whether the leakage current would be higher with a single passivation layer. Therefore, nowhere does Ishaque teach "reducing the lateral leakage current between the plurality of source-drain metal contacts in the high fill factor image array by depositing a second passivation layer over the first passivation layer," as is recited in claims 7, 11, and 16.

The Examiner has stated that "[i]t is noted that depositing the second passivation layer of silicon oxide as taught by AAPA provides the claimed 'reducing the lateral leakage current between the plurality of source/drain metal contacts in the high fill factor image array.'" (Office Action, page 5). However, that is not the case, and the Examiner has not provided further proof for this statement. Embodiments of Applicant's invention provide a two-tier passivation layer where prior-art full fill-factor arrays had a single passivation layer, which as is shown in Figure 4 of the specification (reproduced here as Exhibit D), reduces the lateral leakage current between adjacent optical devices in the array. The Examiner has not shown replacing a single barrier

layer with a two-tiered barrier layer in place of a single barrier layer that reduces the lateral leakage current over that of the single barrier layer acting alone. Ishaque does not teach that the second barrier layer, which is applied to function as a moisture barrier layer, reduces the lateral leakage current over what would be accomplished by a single layer.

In fact, Ishaque specifically teaches that "the organic dielectric is deposited, for example by spin coating, to a thickness of between about 2 microns and about 10 microns; the thickness is selected to provide the desired passivation layer characteristics (except for the moisture resistance) noted above." (Ishaque, col. 5, lines 25-29). The characteristics are the five characteristics desired in the passivating layer: function as an electrically insulating barrier; capable of being selectively etched with respect to the silicon body; covering the photodiode body without cracking or inducing stress; have thickness enough to reduce the internal electric fields; and providing a barrier layer to moisture or chemical attach from environmental exposure. (*See* Ishaque, col. 2, lines 3-31). Consequently, Ishaque teaches that the reduction of leakage current (which is accomplished by the dielectric insulating properties of the layer) is accomplished by the single organic dielectric and the second passivation layer serves only as the moisture barrier.

Therefore, neither the AAPA nor Ishaque, nor their combination, teaches "reducing the lateral leakage current between the plurality of source-drain metal contacts in the high fill factor image array by depositing a second passivation layer over the first passivation layer," as is recited in claims 7, 11, and 16. Furthermore, Possin fails to cure the defects in the teachings of the AAPA and Ishaque. Possin fails to disclose or suggest reducing lateral leakage current by depositing a second passivation layer over a first passivation layer.

2. None of the references teach "reducing the lateral leakage current . . . " and "the second passivation layer being thinner than the first passivation layer."

Claims 7, 11, and 16 each recite "the second passivation layer being thinner than the first passivation layer." None of the references teach this feature.

As illustrated in Figure 3 of the present disclosure, the second passivation layer as recited in claims 7, 11, and 16 is the passivation layer that is closest to the detector silicon. Claim 7 recites "depositing a layer of conductive material over the plurality of source-drain metal contacts and the second passivation layer; depositing a first doped a-Si layer as an optically active layer over the layer of conductive material; patterning the first doped a-Si layer and the layer of conductive material to form collection electrodes." Therefore, as claimed, the optically active layer is deposited over a layer of conductive material which has been deposited over the source-drain metal contact and the second passivation layer.

The opposite is taught in Ishaque, as shown in the Figure, where the thicker layer passivation layer is deposited on the optically active material (material 120) and the thinner passivation layer is deposited on the thicker passivation layer. Although, as discussed above, Ishaque also teaches an embodiment where these two layers are switched, that embodiment results in a higher leakage current. (*See* Ishaque, col. 6, lines 45-51). Therefore, Ishaque does not teach "reducing the lateral leakage current . . . ." and "the second passivation layer being thinner than the first passivation layer."

Similarly, claim 11 recites "depositing a layer of conductive material on the plurality of source-drain metal contacts and over the second passivation layer; depositing a first doped a-Si layer as an optically active layer over the layer of conductive material; patterning the first doped a-Si layer and the layer of conductive material to form collection electrodes," and claim 16 recites "depositing a layer of conductive material on the source-drain metal contact, such that the

layer of conductive material makes electrical contact with the source-drain metal contact; depositing a first doped a-Si layer as an optically active layer on the layer of conductive material; patterning the a-Si layer and the layer of conductive material to form a collection electrode."

The AAPA does not include a second passivation layer at all. Possin does not cure the defects in the teachings of Ishaque and the AAPA.

Therefore, claims 7, 11, and 16, as amended, are allowable over Applicants' prior art, Ishaque, and Possin. Claims 8-10, 12-14, and 17-19, which depend from claims 7, 11, and 16, respectively, are then also allowable over the cited prior art.

II. One skilled in the art would not combine the AAPA, Ishaque, and Possin

As shown in Figure 2 of Applicants specification, the AAPA teaches a full fill-factor array with a passivation layer disposed between optical elements of the array and where the bottom electrode is partially disposed, in a mushroom shape, over the passivation layer. Applicant's claimed invention, as is illustrated in Figure 3 and recited in claims 7, 11, and 16, replaces the single passivation layer with a two-tiered passivation layer (a first passivation layer and a second passivation layer), resulting in a structure with reduced lateral leakage current, as is shown in Figure 4. As is further recited in claims 7, 11, and 16, the first passivation layer and the second passivation layer are both buried within the structure of the device and neither layer is exposed to atmosphere.

Ishaque, however, teaches a structure where a first dielectric layer is deposited to reduce leakage current and a moisture barrier layer is deposited over the first barrier layer in order to prevent contamination of the device from atmospheric exposure. These barrier layers, as is shown in the Figure, are exposed to atmosphere in that structure. One skilled in the art would not recognize a reason to add a moisture barrier layer to the barrier layer taught in the AAPA,

and further would not recognize that doing so would reduce the lateral leakage current over what a single barrier layer already accomplishes.

The passivation layers taught in Ishaque are exposed to atmosphere and Ishaque teaches a second passiviation layer as an atmospheric barrier layer only. One of ordinary skill in the art would not be expected to combine the teachings of Ishaque with that of the AAPA to provide a dual passivation layer.

The Examiner now argues, for the first time, that one skilled in the art would recognize to combine the teachings of Ishaque with AAPA to reduce stress and the resulting cracking in the passivation layers while reducing lateral leakage current. The Examiner states that

> The AAPA discloses on page 2, lines 19-20 that a preferred material for the first passivation layer is silicon oxynitride. The AAPA also discloses on page 3, lines 11-18 that an interface with the silicon oxynitrde and an overlying layer causes conducting channels to occur between two lateral pixel electrodes thus causing lateral leakage. The AAPA further discloses on page 3, lines 19-21 a material different than silicon oxynitride as a passivation layer is advantageous to prevent the conducting channels from forming between two pixel electrodes. Specifically, AAPA teach that one solution to the lateral leakage is to replace the silicon oxynitride passivation layer with silicon oxide at the interface with the a-Si. However, AAPA recognizes that forming the passivation layer of silicon oxide may cause stress build-up that may degrade the sensor structure.

(Office Action, page 4). The Examiner then concludes that "the AAPA recognizes that silicon oxide is advantageous for the passivation layer at the interface with the a-Si to reduce leakage but that it causes stress build-up." *Id.* Further, the Examiner then states that

> Ishaque teaches that one characteristic in a passivation layer is that is [sic] should cover the body without cracking or inducing stresses that adversely effect device performance or the dielectric integrity of the passivating layer (column 2 lines 13-17). Ishaque also teach that single inorganic dielectric layers have been used in some situations but that they cannot be formed to the required thickness

> to provide the desired passivating characteristics without experiencing debilitating stresses that affect the structural integrity of the dielectric layer and degrade device performance (column 2 lines 49-55). However, Ishaque teaches that the dual passivation layer solves these problems by allowing the inorganic dielectric material layer to be relatively thin so that it is not prone to crack or experience significant stress (column 5 lines 57-60 and column 7 lines 32-36).

(Office Action, pgs. 4-5). The Examiner then concludes that

> It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the dual passivation layer of Ishaque in the method of the AAPA in order to use a passivation layer that reduces leakage by having the silicon oxide at the interface with the a-Si and provides the desired thickness without causing stress build-up as taught by Ishaque in column 7 lines 32-42. It is noted that depositing the second passivation layer of silicon oxide as taught by AAPA provides the claimed "reducing the lateral leakage current between the plurality of source/drain metal contacts in the high fill factor image array."

(Office Action, page 5). AS discussed below, the Examiner's analysis is incorrect.

Ishaque clearly teaches that a single polyimide passivation layer can be utilized. As taught in Ishaque "Certain polyimides, particularly preimidized polyimides, have been found to provide a satisfactory passivating layer with regard to several of the desirable characteristics . . . ." (Ishaque, col. 2, lines 33-36). Further, "[t]he organic dielectric is deposited, for example by spin coating, to a thickness of between about 2 microns and about 10 microns; the thickness is selected to provide the desirable passivation layer characteristics (except for the moisture resistance) noted above." (Ishaque, col. 5, lines 25-29). The problem with such layers is that they are susceptible to water damage, and in fact are hydroscopic, which results in the degradation of the device due to increased leakage current. (Ishaque, col. 2, lines 36-44). Clearly this drawback to the use of a single polyimide layer is not a factor where the passivation layer is well buried within the device, as is the case with the device taught in the AAPA. Such a

passivation layer is not exposed to atmosphere and therefore would not suffer damage due to water and other chemical penetration resulting from an exposure to atmosphere. Equally clearly, the device taught in Ishaque suffers damage from water intrusion as a result of exposure of those passivation layers to atmosphere.

Both the AAPA and Ishaque teach that single layer inorganic barrier layers (i.e., oxide or nitride layers) can not be deposited in sufficient thickness to provide dielectric insulation without experiencing debilitating stresses that result in cracking. (*See*, Specification, par. 10 and Ishaque, col. 2, lines 49-55). However, the desire to use such a layer is much different in each case. In the case of Ishaque, a moisture barrier layer is required whereas in Applicant's invention a second barrier layer in contact with the amorphous silicon in order to reduce lateral leakage current is presented.

a. Ishaque teaches away from utilizing its two-tier passivation layer in a structure such as that taught in the AAPA

Ishaque teachs away from replacing the passivation layer illustrated in the AAPA with a two-tiered passivation layer as taught by Ishaque. First, Ishaque teaches that a single polyimide layer is sufficient where moisture is not a problem. Second, Ishaque teaches that placing its inorganic barrier layer on the APD body with the organic barrier layer over the inorganic barrier layer is an inferior solution. Third, Ishaque teaches that deposition of its orgainic dielectric material on amorphous silicon results in contamination of the amorphous silicon.

First, Ishaque teaches that a single polyimide layer is "found to provide a satisfactory passivating layer" in the case where water damage is not an issue. (*See, e.g.,* Ishaque, col. 2, lines 33-36). In the case of the AAPA, water damage is not a problem with the passivation layer being buried deeply within the device, and hence protected from atmospheric exposure by the

remainder of the device. Therefore, Ishaque teaches that the second layer, where exposure to water is not at issue, can be accomplished with a single layer.

Second, from Ishaque's teaching, the alternative embodiment where the inorganic passivation layer was deposited on the APD body and the organic passivation layer deposited over the inorganic layer resulted in higher leakage currents. As stated by Ishaque, "in otherwise similar nine-element arrays, measured leakage current was 10 nA for the arrangement in which the organic dielectric 132 was disposed immediately adjacent to APD body 120, and 30 nA in the embodiment in which the inorganic dielectric was disposed immediately adjacent to APD body 122." (Ishaque, col. 6, lines 45-51). Therefore, Ishaque teaches away from depositing the inorganic barrier layer, its moisture barrier layer, adjacent to the active optical element, the APD. However, in Applicant's invention the intrinsic amorphous silicon is deposited over (and on) the second barrier layer.

Finally, Ishaque teaches away from utilizing amorphous silicon with its barrier layer. (*See* Ishaque, col. 2, line 56-col. 3, line 15). As taught in Ishaque, "in devices in which amorphous silicon comprises the photosensitive semiconductive material, constraints of temperature in the formation process relative to the optimal cure temperature for the polyimide make it undesireable to place the polyimide immediately adjacent to the photosensitive material." (Ishaque, col. 3, lines 2-9). Specifically, Ishaque teaches that the maximum cure temperature of amorphous silicon of about 250 degrees C is well below the temperature required to optimally remove the water contained in the deposited organic layer. Ishaque instead teaches that the "APD body 120 advantageously comprises a photosensitive semiconductive material such as neutron transmutation doped crystalline silicon (typically having less than 0.5% resistivity variation across a wafer) (referred to herein as silicon)." (Ishaque, col. 4, lines 43-47).

Therefore, instead of amorphous silicon devices, such as those described and claimed in Applicant's invention, Ishaque teaches active devices formed of crystalline silicon. Therefore, Ishaque teaches away from utilizing organic layers, such as is taught in Ishaque, in devices with amorphous silicon active materials, such as is recited in Applicant's invention.

For the multiple reasons stated above, one skilled in the art would recognize that passivation layers taught by Ishaque should not be utilized in devices as taught in Applicant's invention.

b. There is no reasonable likelihood of success.

Ishaque teaches providing "moisture-resistant passivation layers adapted for use on arrays of avalanche diodes." (Ishaque, col. 1, lines 10-12). Consequently, Ishaque teaches a passivation "two-tier passivation layer . . . disposed over the APD body so as to cover the outer periphery of the APD body except at a selected contact area with the top contact." (Ishaque, col. 3, lines 42-45). Further, "[t]he passivation layer includes an inorganic moisture barrier layer and an organic dielectric layer." The Examiner contemplates substituting this passivation layer structure for the passivation layer embedded within Applicant's prior art device. In that context, the passivation layer structure would not function as intended by Ishaque et al. In other words, the Examiner contemplates placing a moisture barrier layer embedded within a device where it can not serve its stated function as a moisture barrier layer.

c. Conclusion

For at least the foregoing reasons, Appellant respectfully submits that the Examiner has failed to establish a *prima facie* case of obviousness and that the Board should therefore overturn the Examiner's §103(a) rejection of claims 7-14 and 16-19 from the AAPA in view of Ishaque and Possin. With this rejection overturned, claims 7-14 and 16-19 are allowable.

VIII. Conclusion

For the foregoing reasons, Appellant respectfully requests reversal of all of the bases for rejection set forth in the Issues section above (i.e., Section VI). Please grant any extensions of time required to enter this paper and charge any additional required fees to Deposit Account No. 24-0037.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

By: 
Gary J. Edwards
Reg. No. 41,008

Dated: August 23, 2007

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Appendix A

PENDING CLAIMS

1-6. (Canceled).

7. (Previously presented) A method for making a high fill factor image array comprising the steps:

providing a plurality of source-drain metal contacts on a substrate;

depositing a first passivation layer over the plurality of source-drain metal contacts and the substrate;

reducing the lateral leakage current between the plurality of source-drain metal contacts in the high fill factor image array by depositing a second passivation layer over the first passivation layer, the second passivation layer being thinner than the first passivation layer;

opening a plurality of via holes through the first and second passivation layers to the plurality of source-drain metal contacts;

depositing a layer of conductive material over the plurality of source-drain metal contacts and the second passivation layer;

depositing a first doped a-Si layer as an optically active layer over the layer of conductive material;

patterning the first doped a-Si layer and the layer of conductive material to form collection electrodes;

depositing a continuous layer of i a-Si disposed on the second passivation layer and the first doped a-Si layer;

depositing a continuous second layer of doped a-Si over the continuous layer of i a-Si;

depositing an upper conductive layer over the second layer of doped a-Si; and

patterning to form the image array;

8. (Original) The method for making a high fill factor image array according to claim 7, wherein the first passivation layer comprises silicon oxynitride, BCB, or a polyimide.

9. (Original) The method for making a high fill factor image array according to claim 7, wherein the second passivation layer is an oxide.

10. (Previously presented) The method for making a high fill factor image array according to claim 7, wherein the second passivation layer has a thickness of about 1000 Å.

11. (Previously presented) A high fill factor image array formed by:

providing a plurality of source-drain metal contacts on a substrate;

depositing a first passivation layer over the plurality of source-drain metal contacts and the substrate;

reducing the lateral leakage current between the plurality of source-drain metal contacts in the high fill factor image array by depositing a second passivation layer over the first passivation layer, the second passivation layer being thinner than the first passivation layer;

opening a plurality of via holes through the first and second passivation layers over the plurality of source-drain metal contacts;

depositing a layer of conductive material on the plurality of source-drain metal contacts and over the second passivation layer;

depositing a first doped a-Si layer as an optically active layer over the layer of conductive material;

patterning the first doped a-Si layer and the layer of conductive material to form collection electrodes;

depositing a continuous layer of i a-Si disposed on the second passivation layer and over the first doped a-Si layer;

depositing a continuous second layer of doped a-Si over the continuous layer of i a-Si;

depositing an upper conductive layer over the continuous second layer of doped a-Si; and

patterning to form the image array.

12. (Original) The high fill factor image array of claim 11, wherein the first passivation layer comprises at least one of silicon oxynitride, BCB, or a polyimide.

13. (Original) The high fill factor image array of claim 11, wherein the second passivation layer is an oxide.

14. (Previously presented) The high fill factor image array of claim 11, wherein the second passivation layer has a thickness of about 1000 Å.

15. (Canceled).

16.[1] (Previously presented) A method for making a high fill factor image array comprising:

[1] Although not addressed in this appeal, the Examiner has rejected claim 16 because "the plurality of source-drain metal contacts" has no antecedent basis. This claim will be amended at a later date to substitute -- the source-drain metal contact and an adjacent source-drain metal contact -- for "the plurality of source-drain metal contacts" in the third line of the claim.

providing a source-drain metal contact;

depositing a first passivation layer over the source-drain metal contact;

reducing the lateral leakage current between the plurality of source-drain metal contacts in the high fill factor image array by depositing a second passivation layer over the first passivation layer, the second passivation layer being thinner than the first passivation layer;

opening a via hole through the first and second passivation layers to expose the source-drain metal contact;

depositing a layer of conductive material on the source-drain metal contact, such that the layer of conductive material makes electrical contact with the source-drain metal contact;

depositing a first doped a-Si layer as an optically active layer on the layer of conductive material;

patterning the a-Si layer and the layer of conductive material to form a collection electrode;

depositing sensor material comprising a continuous layer of i a-Si over the collection electrode and at least a portion of the second passivation layer;

depositing a continuous layer of doped a-Si over the continuous layer of i a-Si;

depositing a conductive layer over the continuous layer of doped a-Si; and

patterning conductive layer to form an upper electrode;

17. (Previously presented) The method for making a high fill factor image array according to claim 16, wherein the first passivation layer comprises silicon oxynitride, BCB, or a polyamide.

18. (Previously presented) The method for making a high fill factor image array according to claim 16, wherein the second passivation layer is an oxide.

19. (Previously presented) The method for making a high fill factor image array according to claim 16, wherein the second passivation layer has a thickness of about 1000 Å.

Appendix B

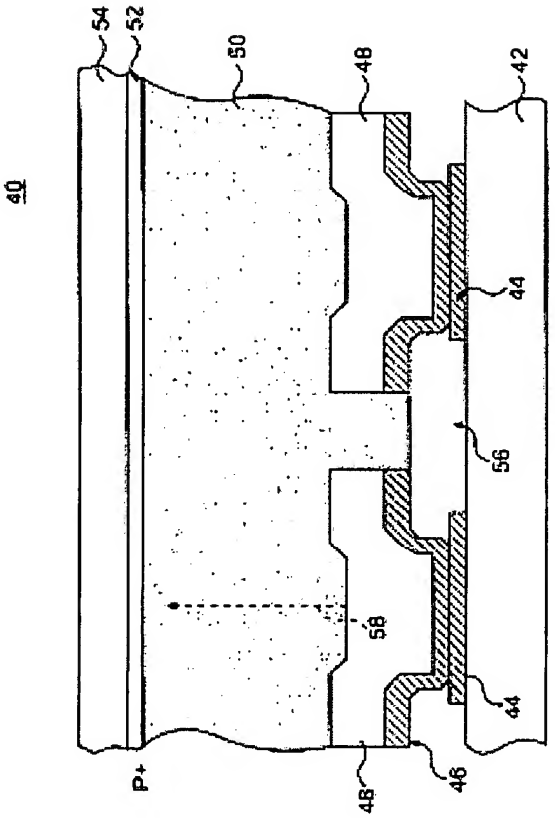

FIG. 2
PRIOR ART

Appendix C

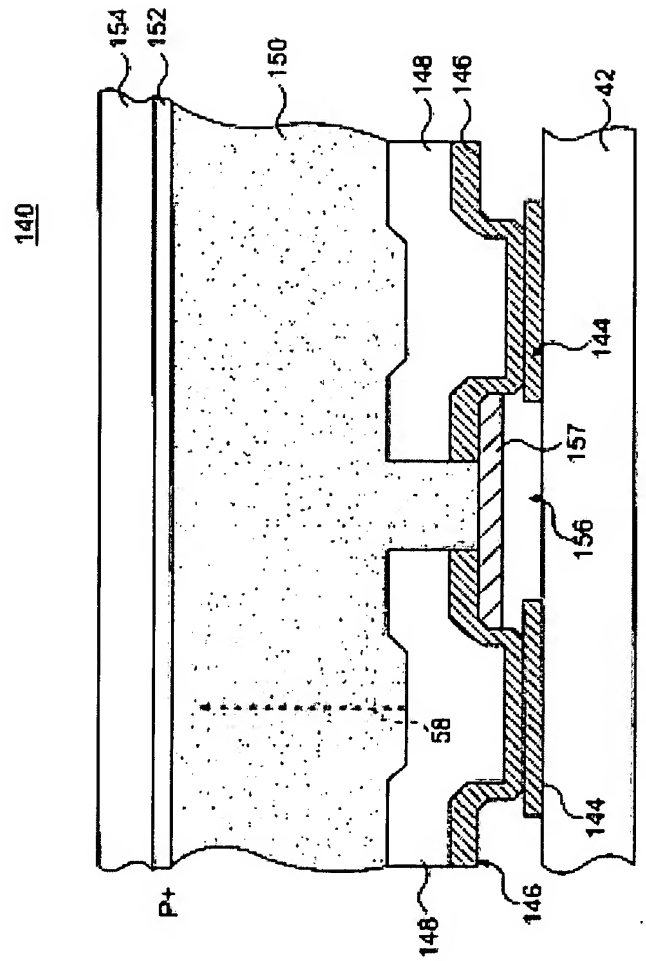

FIG. 3

Appendix D

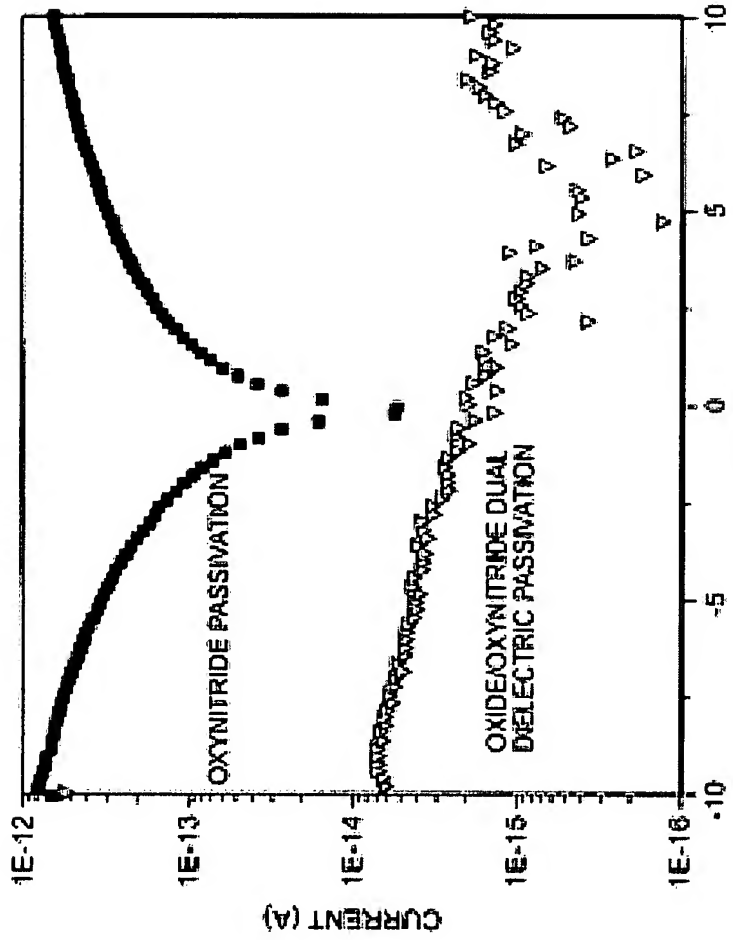

FIG. 4

Appendix E

Evidence Appendix

Evidence Submitted under 37 CFR 1.130, 1.131, or 1.132, or of any other evidence entered by the examiner and relied upon by appelant in the appeal, along with a statement setting forther where in the record that evidence was entered by the examiner under 37 CFR 41.37(c)(1)(ix).

NONE

Appendix F

Related Proceedings

Decisions rendered by a court of the Board in the proceeding identified in the Related Appeals and Interferences section of the brief under 35 CFR 41.37(c)(1)(ix)

NONE